I claim:

1. A semiconductor structure in an integrated circuit, comprising:

an insulating layer on a support;

an interconnect above said insulating layer and separated by a cavity from said insulating layer;

an insulating covering laterally adjoining, in the form of a spacer, said interconnect, said cavity and an upper surface of said interconnect;

said covering having an opening formed therein, extending beyond said interconnect on one side of said interconnect; and

a further insulation layer covering said covering and said opening.

2. The semiconductor structure according to claim 1, wherein said cavity and said interconnect have a substantially equal width.

3. The semiconductor structure according to claim 1, wherein said support has an active region beneath said cavity.

4. The semiconductor structure according to claim 3, wherein said active region is a channel region of a MOS transistor.

5. The semiconductor structure according to claim 1, which comprises a lower conductive layer arranged below a section of said interconnect instead of said cavity.

6. The semiconductor structure according to claim 5, wherein said lower conductive layer is made of doped polysilicon.

7. The semiconductor structure according to claim 1, wherein said cavity is filled with air.

8. The semiconductor structure according to claim 1, wherein said interconnect is composed of a silicide.

9. The semiconductor structure according to claim 1, wherein said insulating layer is composed of silicon oxide.

10. A method of fabricating a semiconductor structure, which comprises:

forming an insulating layer on a support;

applying a lower conductive layer and an upper conductive layer on the insulating layer and patterning the conductive layers in track form;

forming an insulating covering in the form of a spacer on side walls of the lower and upper conductive layers;

producing an opening in the insulating covering, the opening extending beyond the upper conductive layer only on one side of the upper conductive layer and uncovering a surface of the lower conductive layer;

selectively removing the lower conductive layer; and

closing the opening with a further insulating material.

11. The fabrication method according to claim 10, which comprises fabricating the lower conductive layer from doped polysilicon.

12. The fabrication method according to claim 10, which comprises fabricating the upper conductive layer from a silicide.

13. The fabrication method according to claim 10, which comprises removing the lower conductive layer only in sections below the upper conductive layer.

14. The fabrication method according to claim 10, which comprises using KOH in the step of selectively removing the lower conductive layer.

15. The fabrication method according to claim 10, which comprises providing a support with two mutually spaced-apart doped regions of a MOS transistor and thereby producing the cavity above a channel region of the transistor.

16. A method of programming predetermined transistors in an integrated circuit, performing the method according to claim 15 to program predetermined transistors in the integrated circuit.